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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
PATENT APPLICATION

Applicant: Adkisson et al. Serial No.: 10/710879  
Filed: 08/10/2004 Atty. Docket: BUR920040092US1  
Title: DEFECT DIAGNOSIS FOR SEMICONDUCTOR INTEGRATED CIRCUIT.

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**  
**UNDER 37 CFR 1.56, 1.97, 1.98**

Honorable Commissioner of Patents and Trademarks  
Washington, D. C. 20231

Sir:

Applicants submit herewith form PTO-1449, listing patents, publications, or other information of which they are aware which they believe may be material to patentability pursuant to 37 CFR 1.56(b), and in respect of which there may be a duty to disclose under 37 CFR 1.56(a), together with legible copies of the patents, publications, or other information listed.

While the items submitted with this Information Disclosure Statement may be material to patentability pursuant to 37 CFR 1.56, in accordance with 37 CFR 1.97(h) it shall not be construed to be an admission that any patent, publication, or other information cited is "prior art" or is material to patentability for this invention unless specifically designated as such. In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other information material to patentability, as defined in 37 CFR 1.56(b), exists.

Respectfully submitted,

Date: Aug 13, 2004

By:

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## INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)

BUR920040092US1

Application Number

10/710879

Applicant(s)

Adkisson et al.

Filing Date

08/10/2004

Group Art Unit

## U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

## U.S. PATENT APPLICATION PUBLICATIONS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

## FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO
		014661	12/1986	EPO				

## OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

		K. W. Lallier et al., RELATING LOGIC DESIGN TO PHYSICAL GEOMETRY IN LSI CHIP, Vol. 19, No. 6, November 1976, pages 2140-2143.

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.